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PeakSHDSL 8 CHANNEL CENTRAL OFFICE CHIPSET

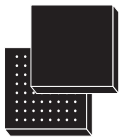
PRODUCT BRIEF

DESCRIPTION

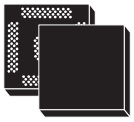
The 8-channel SHDSL chipset from STMicroelectronics provides a complete low-power, low cost solution for Central Office (CO) SHDSL solutions. The chipset integrates all SHDSL functions from Utopia interface to the line in three devices:

- STLC80815: 8 channel SHDSL data pump (SHDSL Transceiver)
- STLC60444: 4 channel SHDSL Analog front end
- TS615: Dual wide band operational amplifier with high output current

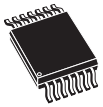
The product is targeted for customers looking to build cost effective central office solutions, including Digital Subscriber Line Access Multiplexers (DSLAM) and Digital Loop Carriers (DLC).



PBGA-272 package for STLC80815 device



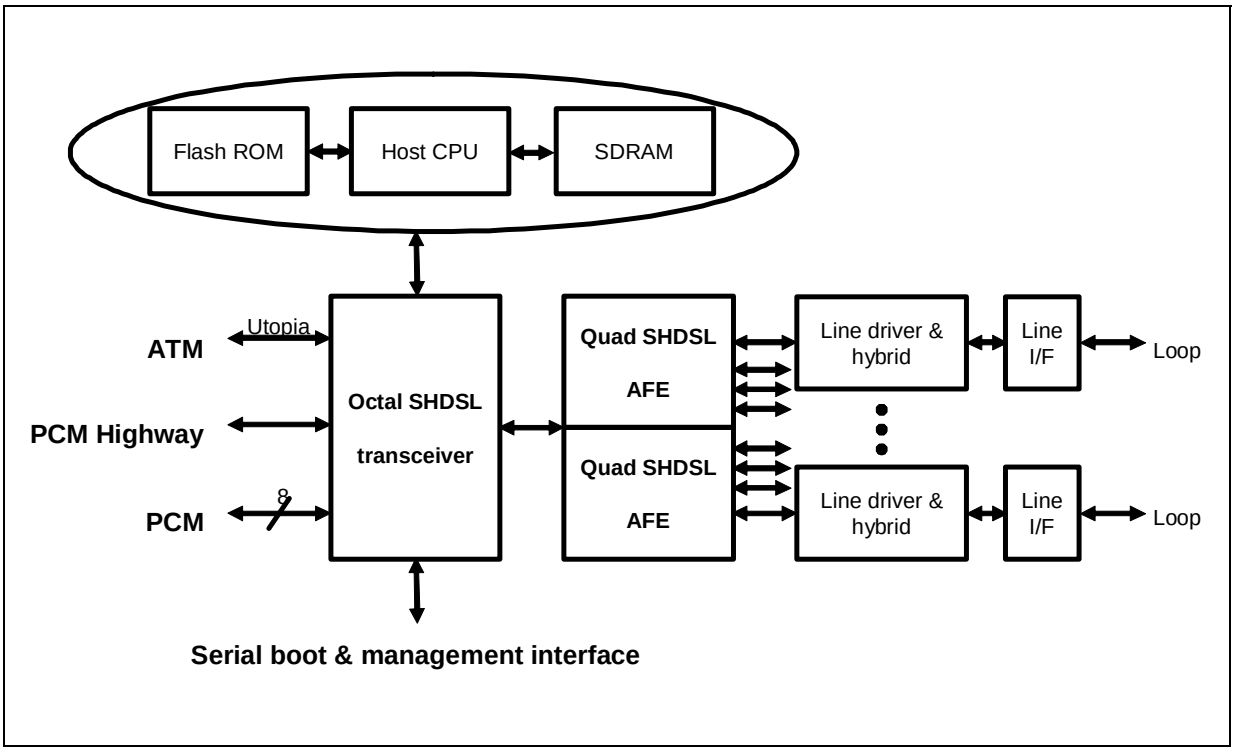
EFBGA216 package for STLC60444 device



TSSOP14 package for TS615 device

CHIPSET ARCHITECTURE OVERVIEW

Figure 1. Chipset Architecture Overview



With less than 750 mWatt per channel, the PeakSHDSL chipset is one of the most competitive solutions for SHDSL central office applications.

This is preliminary information on a new product now in development. Details are subject to change without notice.

STLC80815- 8 CHANNEL SHDSL DATA PUMP (SHDSL TRANSCEIVER)

Introduction

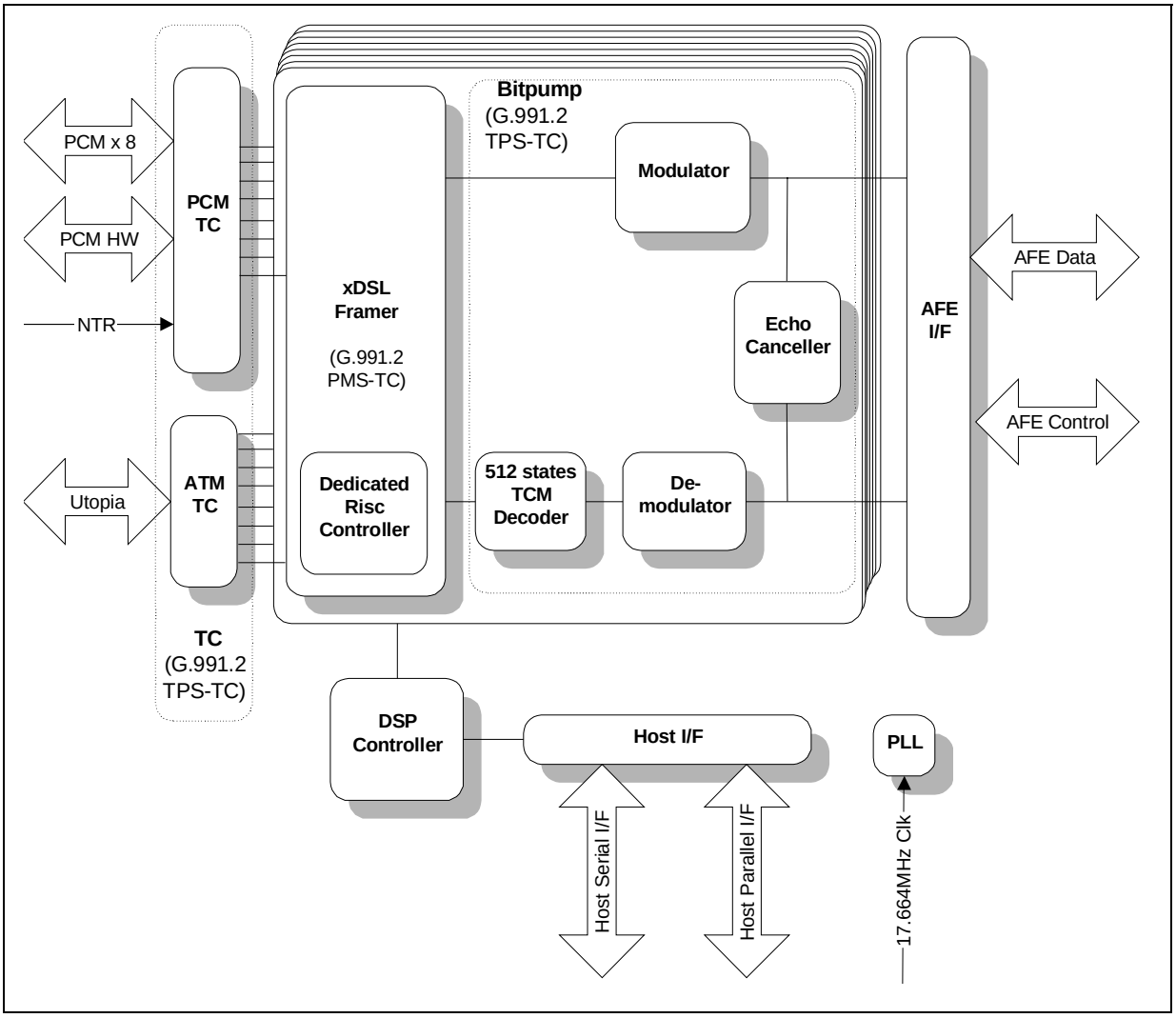
The STLC80815 includes eight independent transceivers, which are optimized for central office application of Symmetrical Digital Subscriber Line (SHDSL) modems. The channels can operate simultaneously in different modes and standards. It is an ideal integrated solution for central office equipment sensitive to cost, power and space.

It includes full object code for a complete management/control and diagnostic API, and requires only power up initialization from the host interface. This allows a single low-cost host processor to supports tens of ports via a parallel or serial interface.

A "hostless" line card can be designed using the STLC80815. In this case a remote host can boot the chip and manage it via a serial host interface or using the in-band ATM cells.

Each channel in this highly integrated device includes the following components: frame, a PAM receiver and transmitter, a 512 state TCM decoder and a timing synthesizer. In addition the device includes a centralized controller, which reduces to a minimum the requirements placed from the host, a Utopia and a PCM highway interface, which are common to all eight channels.

Figure 2. Block diagram of the STLC80815 SHDSL transceiver



Main features

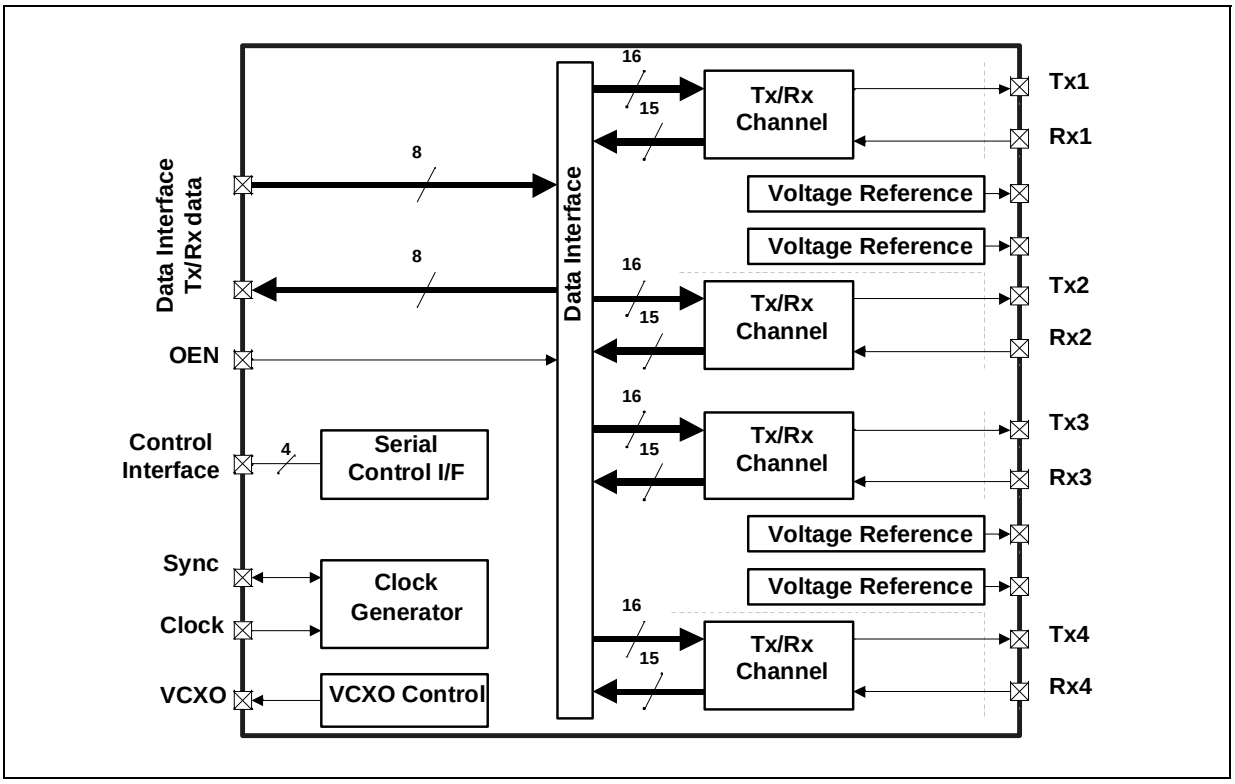
- Compatibility with: ITU G.991.2 (G.SHDSL), ITU G.994.1 (G.HS) and ETSI RE/TM-06011 (SDSL), ANSI HDSL2 and HDSL4.
- Supports four-wire operation
- Extremely low power consumption per channel: <700mW for all ITU G.991.2 Annex B rates, masks and loops.
- Outstanding reach performance: Symmetrical rate of 1552kbps over 5.5 Km (18.0kft) for an ETSI 0.4mm cable.
- Includes 512 states TCM decoder
- Supports symmetrical rates from 192 kbps up to 2.3 Mbit/s in step of 8kbps
- Includes an internal, flexible frequency synthesizer
- Supports all G.991.2 clock modes, including synchronous and plesiochronous modes.
- Support operation with NTR, External PLL or VCXO are not required
- Includes a fully-featured flexible framer, which supports simultaneous ATM and PCM transmission
- T1/E1 and in-band ISDN services are supported
- Serial and parallel host interface
- In-band ATM boot and management supported
- Complete software control protocol stack/API
- Boundary scan testing compliant to IEEE 1149.1 Join Test Action Group (JTAG)
- 272-pin TPBGA272 package (27x27mm)
- -40 to 85°C operation

STLC60444- 4-CHANNEL SHDSL ANALOG FRONT END

Short introduction

The STMicroelectronics STLC60444 Quad AFE incorporates four complete analog front ends, optimized for Central Office (CO) ADSL and SHDSL modems. The device integrates high-resolution analog to digital converters (ADC) and digital to analog converters (DAC), which combined with active filtering significantly reduces the requirements placed on external components. The STLC60444 Quad AFE is ideal for cost, power and board area sensitive CO equipment.

Figure 3. Block diagram of STLC60444 SHDSL Analog Front End



Main features

- Integrates four complete full-rate ADSL/SHDSL analog front ends
- Integrates all active circuits except transmit line drivers
- Low power, 3.3V operation
- Integrated analog filters and 15-bit A/D & D/A converters
- Interpolation filtering to reduce transmit channel data rate
- 0 to +48 dB PGA range for each receive channel
- Excellent SFDR and input noise performance
- 0.35µm CMOS technology with Triple Well
- Industrial temperature range (-40 °C to +85 °C)

TS615 - DUAL WIDE BAND OPERATIONAL AMPLIFIER WITH HIGH OUTPUT CURRENT

Short Introduction

The TS615 is a dual operational amplifier featuring a high output current 410mA. The TS615 is ideally suited for xDSL applications. The device is designed for the high slew rates to support low harmonic distortion and intermodulation.

Main features

- Low Noise: 5.2nV/(Hz)$^{1/2}$
- High Peak Output Current: 420mA
- Very Low Harmonic and Intermodulation Distortion (IM2 = -86dBc)
- High Slew Rate: 410V/µsec
- Current Feedback Structure
- 14 pins TSSOP package

PeakSHDSL OCTAL-QUAD EVALUATION BOARD

ST offers a 8-channel evaluation board (EVM) which includes the STLC80815 eight-port SHDSL DSP, two STLC60444 four-port AFE, eight line drivers, channel interface and protection circuits. The board is available now.

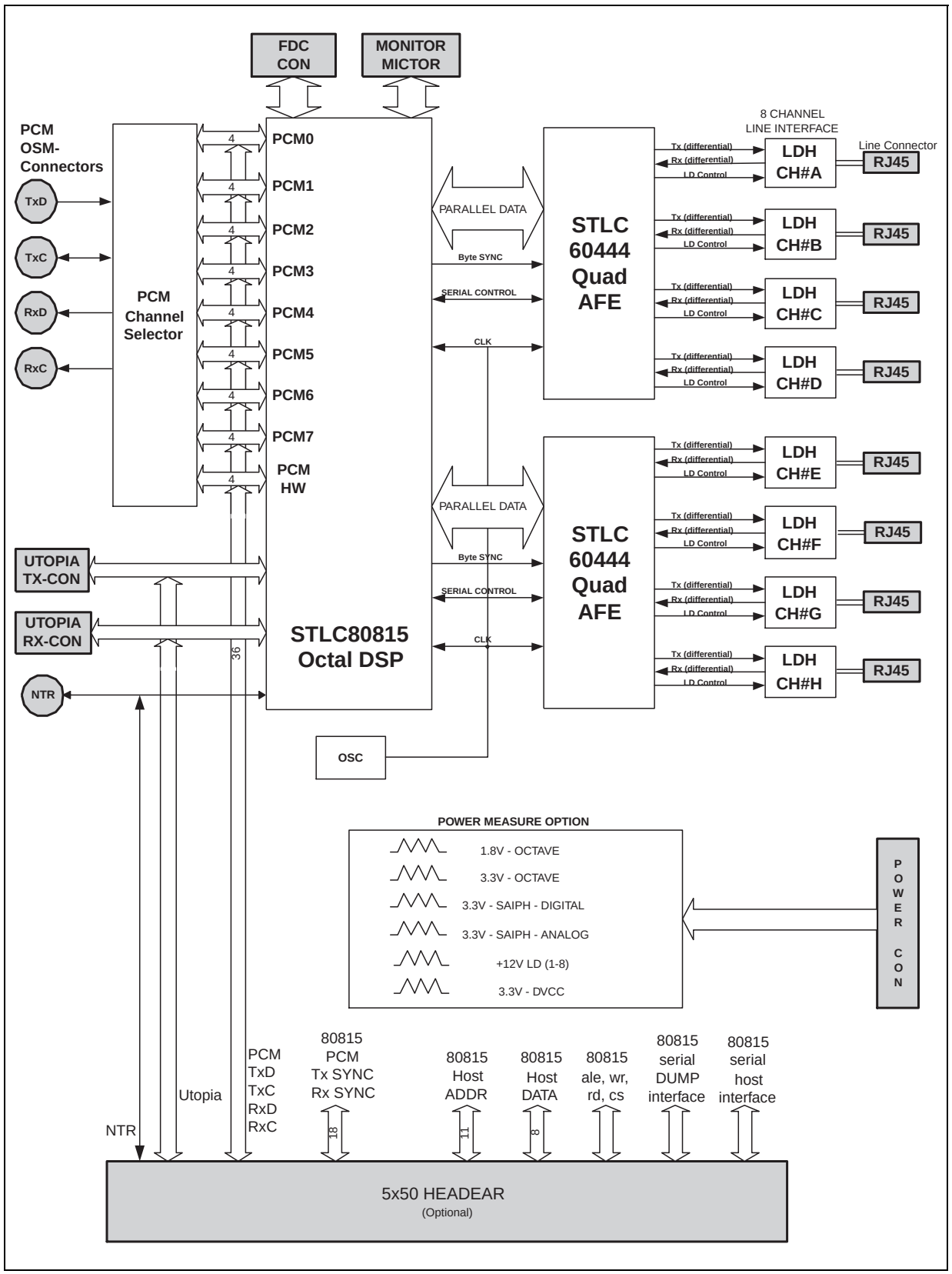
The board includes the following Interfaces:

- FDC interface (see below)
- Two UTOPIA connectors
- PCM OSM connectors, which can be multiplexed to a selected channel.
- OSM NTR
- 5x50 Header, which is connected to various points in the circuit, including all the PCM channels
- Eight RJ45 connectors to the lines

The board uses +12V, 3.3V and 1.8V supply rails.

For your reference the block diagram of the board is provided below:

Figure 4. Block Diagram of the PeakSHDSL Octal-Quad EVM



OCTAL CHIPSET, SOFTWARE AND REFERENCE DESIGN

The PeakSHDSL chipset consists of an octal digital Transceiver (STLC80815) and two quad AFEs (STLC60444). These chips are part of a chipset with a number of user interfaces available including Utopia level 2, Eight PCM (16 for the Hex solution), and PCM highway.

Software and Management is supported through:

- A complete software control protocol stack/API
- No need for real-time interaction with any host CPU
- Supports in-band ATM management and in-band boot through the Utopia interface
- Hostless line-card design using serial host i/f or in-band ATM
- Boundary scan testing compliant to IEEE 1149.1 Joint Test Action Group (JTAG)

The PeakSHDSL solution is provided via a fully documented, turnkey transceiver reference design, development systems, and technical support. This includes a development kit that allows customers to shorten the designer's development time by quickly building complete SHDSL solutions:

- **A Hardware Design Guide** - which includes transceiver schematics, transceiver layout gerbers and bill of materials (BOM). The design guide also includes details on planning, layout, testing and debugging an SHDSL product.
- **A Software Design Guide** - which includes a detailed description of the management protocol. Moreover, ST offers the Host CPU Interface Library software code with instructions to help integrate the software functions into the customer's source code.
- **Fast Debugger Card (FDC) and Manager Analyzer Tools** - To assist customers with evaluation, test and debug of their SHDSL design at the early phase of development, ST offers the Fast Debugger Card (FDC) and Manager Analyzer Tools (OMANA, a MS-Windows® based PC application). Using these tools enables testing the SHDSL circuitry even before the host controller software is completed, by bypassing the host using the FDC. The Manager Analyzer Tool enables the customer to configure the SHDSL transceiver and test performance and provides a graphic display of system performance.
- **The Profiler** - to assist incorporating the interface library into the host software, ST provides the Profiler. The Profiler is a PC based application that displays statistics on memory and real time requirements of the API task, the interrupt handler and the messages queues that are used. Using this tool will scale the required memory buffers and help identify and solve real time issues during software integration.

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